

# CD4532B Types

## CMOS 8-Bit Priority Encoder

### High-Voltage Types (20-Volt Rating)

■ CD4532B consists of combination logic that encodes the highest priority input (D7-D0) to a 3-bit binary code. The eight inputs, D7 through D0, each have an assigned priority; D7 is the highest priority and D0 is the lowest. The priority encoder is inhibited when the chip-enable input  $E_I$  is low. When  $E_I$  is high, the binary representation of the highest-priority input appears on output lines Q2-Q0, and the group select line GS is high to indicate that priority inputs are present. The enable-out ( $E_O$ ) is high when no priority inputs are present. If any one input is high,  $E_O$  is low and all cascaded lower-order stages are disabled.

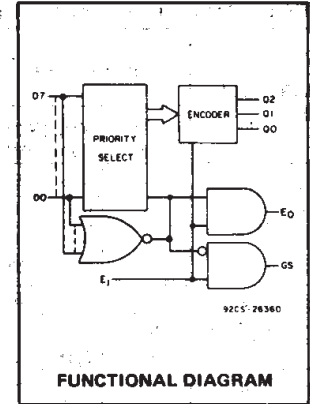
The CD4532B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

### Features:

- Converts from 1 of 8 to binary
- Provides cascading feature to handle any number of inputs
- Group select indicates one or more priority inputs
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of  $1 \mu\text{A}$  at 18 V over full package temperature range;  $100 \text{ nA}$  at 18 V and  $25^\circ\text{C}$
- Noise margin (full-package-temperature range):
  - 0.5 V at  $V_{DD} = 5 \text{ V}$
  - 1.5 V at  $V_{DD} = 10 \text{ V}$
  - 1.5 V at  $V_{DD} = 15 \text{ V}$
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

### Applications:

- Priority encoder
- Binary or BCD encoder (keyboard encoding)
- Floating point arithmetic



### RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	Min.	Max.	Units
Supply Voltage Range (for $T_A =$ Full Package Temp. Range)	3	18	V

### MAXIMUM RATINGS, Absolute-Maximum Values:

#### DC SUPPLY-VOLTAGE RANGE, ( $V_{DD}$ )

Voltages referenced to  $V_{SS}$  Terminal .....  $-0.5\text{V}$  to  $+20\text{V}$

INPUT VOLTAGE RANGE, ALL INPUTS .....  $-0.5\text{V}$  to  $V_{DD} + 0.5\text{V}$

DC INPUT CURRENT, ANY ONE INPUT .....  $\pm 10\text{mA}$

#### POWER DISSIPATION PER PACKAGE ( $P_D$ ):

For  $T_A = -55^\circ\text{C}$  to  $+100^\circ\text{C}$  .....  $500\text{mW}$

For  $T_A = +100^\circ\text{C}$  to  $+125^\circ\text{C}$  ..... Derate Linearly at  $12\text{mW}/^\circ\text{C}$  to  $200\text{mW}$

#### DEVICE DISSIPATION PER OUTPUT TRANSISTOR

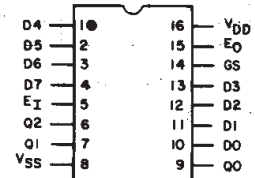
FOR  $T_A =$  FULL PACKAGE-TEMPERATURE RANGE (All Package Types) .....  $100\text{mW}$

OPERATING-TEMPERATURE RANGE ( $T_A$ ) .....  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$

STORAGE TEMPERATURE RANGE ( $T_{stg}$ ) .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$

#### LEAD TEMPERATURE (DURING SOLDERING):

At distance  $1/16 \pm 1/32$  inch ( $1.59 \pm 0.79\text{mm}$ ) from case for 10s max .....  $+285^\circ\text{C}$



(TOP VIEW)

92CS-24596R1

### TERMINAL ASSIGNMENT

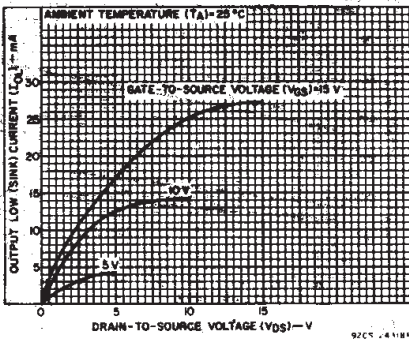


Fig. 1 - Typical output low (sink) current characteristics.

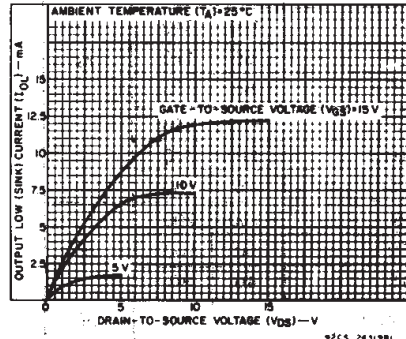


Fig. 2 - Minimum output low (sink) current characteristics.

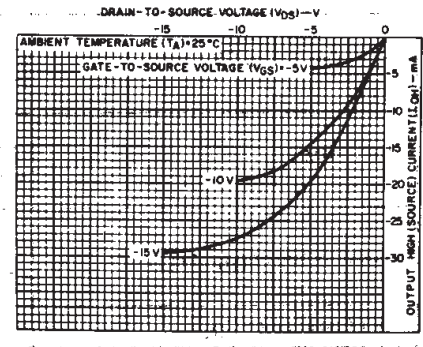


Fig. 3 - Typical output high (source) current characteristics.

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## STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V <sub>O</sub> (V)	V <sub>IN</sub> (V)	V <sub>DD</sub> (V)	-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current, I <sub>DD</sub> Max.	-	0,5	5	5	5	150	150	-	0,04	5	μA
	-	0,10	10	10	10	300	300	-	0,04	10	
	-	0,15	15	20	20	600	600	-	0,04	20	
	-	0,20	20	100	100	3000	3000	-	0,08	100	
Output Low (Sink) Current I <sub>OL</sub> Min.	0,4	0,5	5	0,64	0,61	0,42	0,36	0,51	1	-	mA
	0,5	0,10	10	1,6	1,5	1,1	0,9	1,3	2,6	-	
	1,5	0,15	15	4,2	4	2,8	2,4	3,4	6,8	-	
Output High (Source) Current, I <sub>OH</sub> Min.	4,6	0,5	5	-0,64	-0,61	-0,42	-0,36	-0,51	-1	-	mA
	2,5	0,5	5	-2	-1,8	-1,3	-1,15	-1,6	-3,2	-	
	9,5	0,10	10	-1,6	-1,5	-1,1	-0,9	-1,3	-2,6	-	
	13,5	0,15	15	-4,2	-4	-2,8	-2,4	-3,4	-6,8	-	
Output Voltage: Low-Level, V <sub>OL</sub> Max.	-	0,5	5	0,05			-	0	0,05	-	V
	-	0,10	10	0,05			-	0	0,05	-	
	-	0,15	15	0,05			-	0	0,05	-	
Output Voltage: High-Level, V <sub>OH</sub> Min.	-	0,5	5	4,95			4,95	5	-	-	V
	-	0,10	10	9,95			9,95	10	-	-	
	-	0,15	15	14,95			14,95	15	-	-	
Input Low Voltage, V <sub>IL</sub> Max.*	0,5, 4,5	-	5	1			-	-	1,5	-	V
	1,9	-	10	2,5			-	-	3	-	
	1,5, 13,5	-	15	3			-	-	4	-	
Input High Voltage, V <sub>IH</sub> Min.*	0,5, 4,5	-	5	4			3,5	-	-	-	V
	1,9	-	10	7,5			7	-	-	-	
	1,5, 13,5	-	15	12			11	-	-	-	
Input Current I <sub>IN</sub> Max.		0,18	18	±0,1	±0,1	±1	±1	-	±10 <sup>-5</sup>	±0,1	μA

\*One input is tested at a time; other inputs should be at V<sub>DD</sub> or V<sub>SS</sub>. For testing all inputs at V<sub>IL</sub> and V<sub>IH</sub> levels, use 20%/80% V<sub>DD</sub>.

## DYNAMIC ELECTRICAL CHARACTERISTICS at T<sub>A</sub>=25°C; C<sub>L</sub>=50 pF, Input t<sub>r</sub>, t<sub>f</sub>= 20 ns, R<sub>L</sub>=200 kΩ

CHARACTERISTIC	TEST CONDITIONS V <sub>DD</sub> VOLTS	LIMITS		UNITS
		TYP.	MAX.	
Propagation Delay Time t <sub>PHL</sub> , t <sub>PLH</sub> E <sub>I</sub> to E <sub>O</sub> , E <sub>I</sub> to G <sub>S</sub>	5	110	220	ns
	10	55	110	
	15	45	85	
E <sub>I</sub> to Q <sub>m</sub> , D <sub>n</sub> to G <sub>S</sub>	5	170	340	ns
	10	85	170	
	15	65	125	
D <sub>n</sub> to Q <sub>M</sub>	5	220	440	ns
	10	110	220	
	15	85	160	
Transition Time t <sub>THL</sub> , t <sub>TLH</sub>	5	100	200	ns
	10	50	100	
	15	40	80	
Input Capacitance C <sub>IN</sub>	Any Input	5	7,5	pF

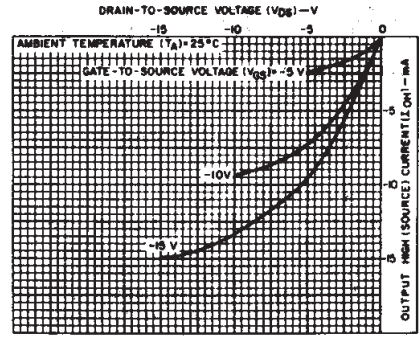


Fig. 4 - Minimum output high (source) current characteristics.

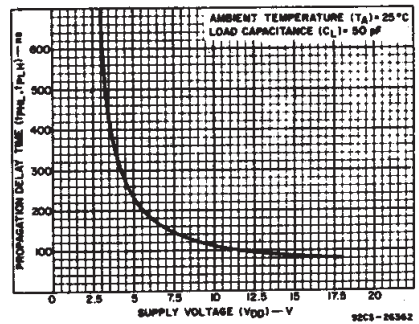


Fig. 5 - Typical propagation delay (D<sub>n</sub> to Q<sub>m</sub>) vs. supply voltage.

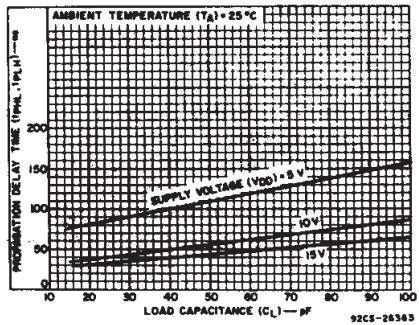


Fig. 6 - Typical propagation delay (E<sub>I</sub> to G<sub>S</sub>, E<sub>I</sub> to E<sub>O</sub>) vs. load capacitance.

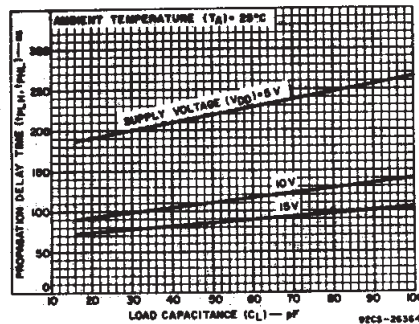
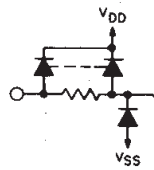
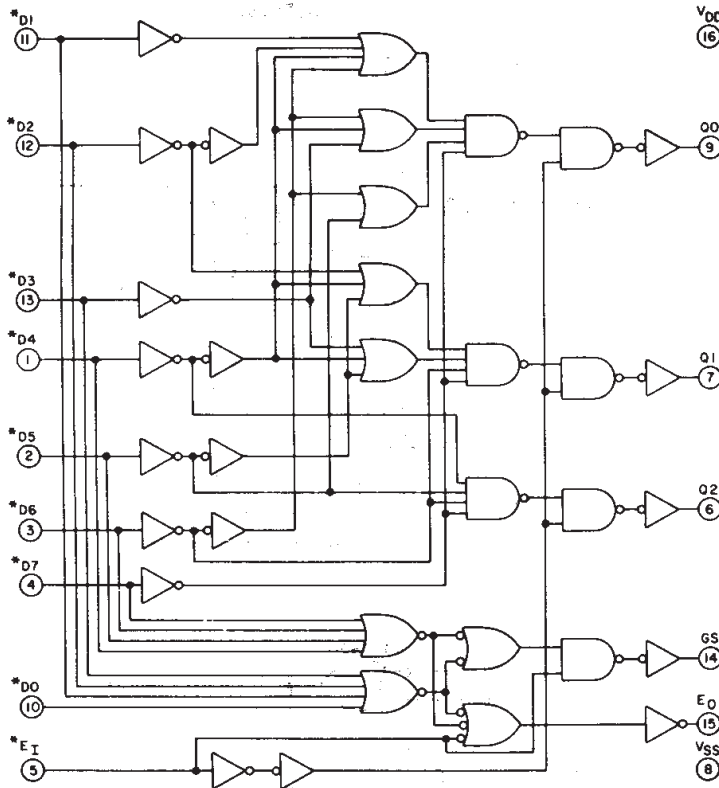


Fig. 7 - Typical propagation delay (D<sub>n</sub> to Q<sub>m</sub>) vs. load capacitance.

# CD4532B Types



\*ALL INPUTS PROTECTED BY CMOS PROTECTION NETWORK

Fig. 8 - CD4532 logic diagram.

## TRUTH TABLE

Input									Output				
E <sub>I</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	G <sub>S</sub>	Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>	E <sub>O</sub>
0	X	X	X	X	X	X	X	X	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	1
1	1	X	X	X	X	X	X	X	1	1	1	1	0
1	0	1	X	X	X	X	X	X	1	1	1	0	0
1	0	0	1	X	X	X	X	X	1	1	0	1	0
1	0	0	0	1	X	X	X	X	1	1	0	0	0
1	0	0	0	0	1	X	X	X	1	0	1	1	0
1	0	0	0	0	0	1	X	X	1	0	1	0	0
1	0	0	0	0	0	0	1	X	1	0	0	1	0
1	0	0	0	0	0	0	0	1	1	0	0	0	0

X = Don't Care

Logic 1 ≡ High

Logic 0 ≡ Low

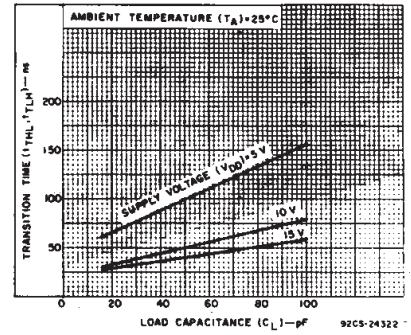


Fig. 9 - Typical transition time vs. load capacitance.

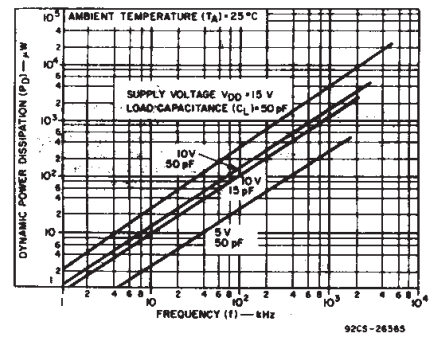


Fig. 10 - Typical dynamic power dissipation vs. frequency.

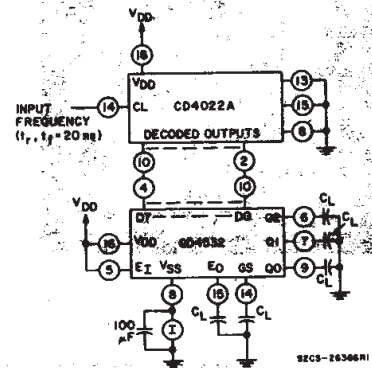


Fig. 11 - Dynamic power dissipation test circuit.

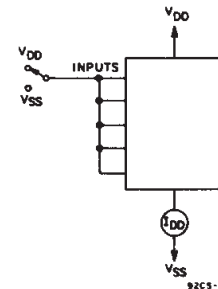


Fig. 12 - Quiescent device current test circuit.

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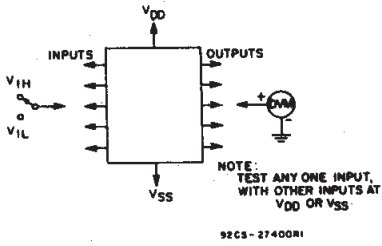


Fig. 13 - Input voltage test circuit.

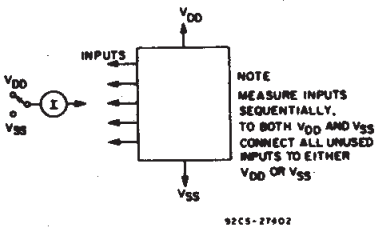
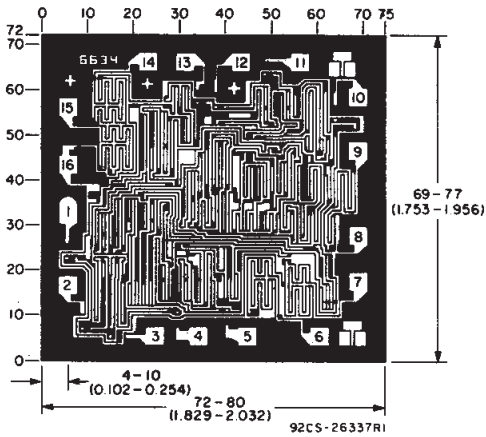


Fig. 14 - Input current test circuit.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

Dimensions and pad layout for CD4532BH.

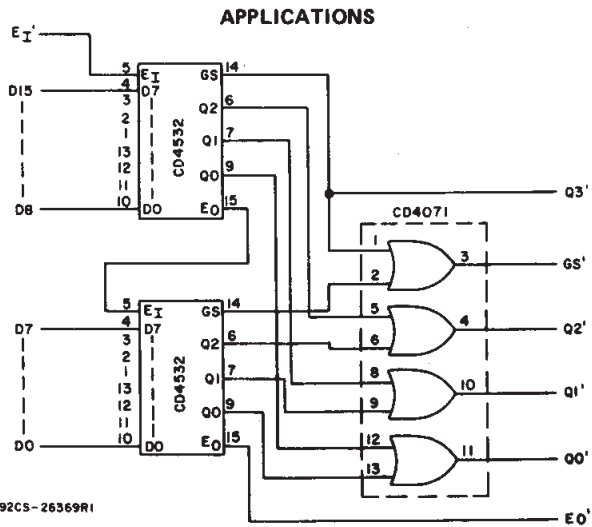
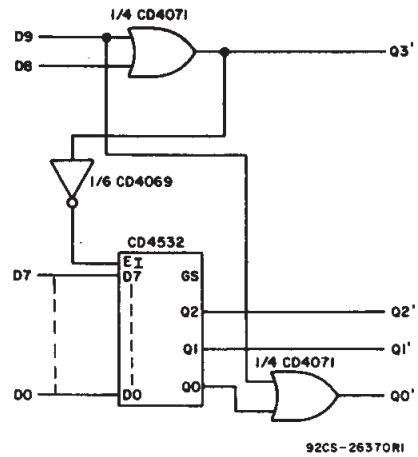


Fig. 15 - 16-level priority encoder.



## TRUTH TABLE

Input									Output					
D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	GS	Q3'	Q2'	Q1'	Q0'
1	X	X	X	X	X	X	X	X	X	0	1	0	0	1
0	1	X	X	X	X	X	X	X	X	0	1	0	0	0
0	0	1	X	X	X	X	X	X	X	1	0	1	1	1
0	0	0	1	X	X	X	X	X	X	1	0	1	1	0
0	0	0	0	1	X	X	X	X	X	1	0	1	0	1
0	0	0	0	0	1	X	X	X	X	1	0	1	0	0
0	0	0	0	0	0	1	X	X	X	1	0	0	1	1
0	0	0	0	0	0	0	1	X	X	1	0	0	1	0
0	0	0	0	0	0	0	0	1	X	1	0	0	0	1
0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

X = Don't Care

Logic 1  $\equiv$  High

Logic 0  $\equiv$  Low

Fig. 16 - 0-to-9 keyboard encoder.

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