ACL-7124

24-Bit Parallel
Digital I/O Board

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Product Warranty/Service

How to Use This Guide

This manual is designed to help you use the ACL–7124. The manual describes how to modify various settings on the ACL–7124 card to meet your requirements. It is divided into three chapters:

- Chapter 1, "Introduction," gives an overview of the product features, applications, and specifications.

- Chapter 2, "Installation," describes how to install the ACL–7124. The layout of ACL–7124 is shown, the DIP switch setting for base address, and jumper settings for IRQ level and interrupt status are specified.

- Chapter 3, "Programming," describes how to program the digital input and output ports on the ACL–7124.

- Appendix A, " I/O Port Address Map", specifies the PC's default I/O Port address map.

1

Introduction

The ACL-7124 : 24-bit Digital I/O board is a parallel Digital I/O board for IBM PC/XT/AT or compatibles in industrial applications. It is fully hardware and software compatible with Advantech PCL-724.

This board emulates one industry standard 8255 Programmable Peripheral Interface (PPI) chip, it offers 3 ports: PA, PB, and PC. The PC can also be subdivided into 2 nibble-wide (4-bit) ports - PC Upper and PC Low. One 50-pin male ribbon connector comes equipped with the ACL-7124. In addition, two 20-pin connectors, which are corresponding to the 50-pin connector, are also supported for 16-bit digital I/O daughter boards, such as ACLD-782 and ACLD-785.

The ACL-7124 is programmed using simple 8-bit I/O port commands (*inport and outport*) or an ACLS-DLL1: digital I/O software driver for high level C language or Windows applications.

1.1 Features

The ACL-7124 24-Bit Parallel Digital I/O Board provides the following advanced features:

- 24 TTL/DTL compatible digital I/O lines

- Emulates one industry standard mode 0 of 8255 PPI

- Buffered circuits for higher driving

- Direct interface with OPTO-22 compatible I/O module

- Programmable interrupt handling

- Output status readback

- Fully hardware and software compatible with Advantech PCL-7124

1.2 Applications :

- Programmable mixed digital input & output

- Industrial monitoring and control

- Digital I/O control

- Contact closure, switch/keyboard monitoring

- Connects with OPTO-22 compatible modules

- Useful with A/D and D/A to implement a data acquisition & control system

1.3 Specifications:

I/O channels	24
Input Signal	Logic High Voltage :2.0 V to 5.25V Logic Low Voltage : 0.0 V to 0.80V Logic High Current : 20.0 uA Logic Low Current : −0.2 mA
Output Signal	Logic High Voltage : Minimum 2.4 V Logic Low Voltage : Maximum 0.5V Logic High Current : −15.0 mA Logic Low Current : 24.0 mA
Operating Temperature	0° ~ 60° C
Storage Temperature	−20° ~ 80° C
Humidity	5% ~ 95% non−condensing
I/O Connector	50−pin male ribbon cable connector
Bus	PC/XT Bus
IRQ Level	IRQ2 ~ IRQ7
I/O port address	4 bytes(Hex 200 ~ Hex 3FF)
Power Consumption	0.5A @5VDC (Typical) 0.8A @5VDC (Maximum)
Transfer Rate	300 K bytes/sec (Typical) 500 K bytes/sec (Maximum)
Size	(110mm X 97mm)

2

Installation

This chapter describes how to install the ACL-7124. At first, the contents in the package and unpacking information that you should be careful are described. The DIP switch and jumper settings for the ACL-7124's base address, interrupt IRQ level and interrupt mode and status are also specified.

2.1   What You Have

In addition to this *User's Manual*, the package includes the following items:

- ACL-7124 24-bit Parallel Digital I/O Card
- Manual & Software Utility CD

If any of these items is missing or damaged, contact the dealer from whom you purchased the product. Save the shipping materials and carton in case you want to ship or store the product in the future.

2.2   Unpacking

Your ACL-7124 card contains sensitive electronic components that can be easily damaged by static electricity.

The card should be done on a grounded anti-static mat. The operator should be wearing an anti-static wristband, grounded at the same point as the anti-static mat.

Inspect the card module carton for obvious damage. Shipping and handling may cause damage to your module. Be sure there are no shipping and handing damages on the module before processing.

After opening the card module carton, exact the system module and place it only on a grounded anti-static surface component side up.

Again inspect the module for damage. Press down on all the socketed IC's to make sure that they are properly seated. Do this only with the module place on a firm flat surface.

Note : DO NOT APPLY POWER TO THE CARD IF IT HAS BEEN
          DAMAGED.

You are now ready to install your ACL-7124.

2.3 ACL-7124's Layout
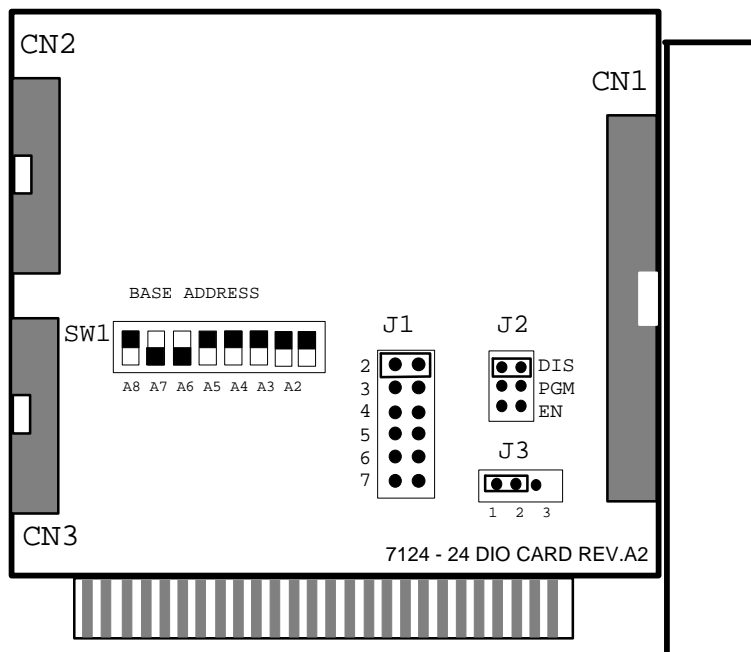
Figure 2.1 ACL-7124's Layout

2.4   Jumper and DIP Switch Description

You can change the ACL-7124's base address and interrupt by setting DIP switches and jumpers on the card. The card's jumpers and switches are preset at the factory. Under normal circumstances, you should not need to change the jumper settings.

A jumper switch is closed (sometimes referred to as "shorted" with the plastic cap inserted over two pins of the jumper). A jumper is open with the plastic cap inserted over one or no pin(s) of the jumper.

2.5   Base Address Setting

The ACL-7124 requires 4 consecutive address locations in I/O address space. The base address of the ACL-7124 is restricted by the following conditions.

   1. The base address must be within the range Hex 200 to Hex 3FF.

   2. The base address should not conflict with any PC reserved I/O address. (refer to Appendix A)

The address setting of the ACL-7124 is described in Table 2.3.

SW1:   BASE ADDR = 0x 2C0.
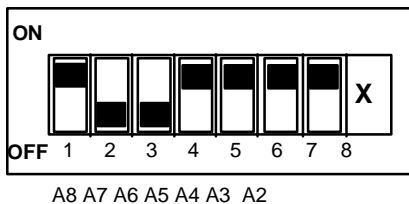
Figure 2.3 Default DIP switch setting

I/O port address(hex)	1 A8	2 A7	3 A6	4 A5	5 A4	6 A3	7 A2	8 --
200-203	0 (ON)	1 (ON)	1 (ON)	0 (ON)	0 (ON)	0 (ON)	0 (ON)	X
⋮ ⋮								
(*) 2C0-2C3	0 (ON)	1 (OFF)	1 (OFF)	0 (ON)	0 (ON)	0 (ON)	0 (ON)	X
⋮ ⋮								
3F8-3FB	1 (OFF)	1 (OFF)	1 (OFF)	1 (OFF)	1 (OFF)	1 (OFF)	0 (ON)	X
3FC-3FF	1 (OFF)	1 (OFF)	1 (OFF)	1 (OFF)	1 (OFF)	1 (OFF)	1 (OFF)	X

(*) : default setting
X   : Don't care
ON = 0 ; OFF = 1
A2, ..., A8 are corresponding to address lines of ISA bus.
A9 is always **1** (OFF).

Table 2.1 Base Address Table

How to Define a Base Address for the ACL-7124 ?

The DIP1 to DIP7 in the switch SW1 are one to one corresponding to the PC bus address line A8 to A2. A9 is always 1; A1 and A2 are always 0. If you want to change the base address, you can only change the values of A2 to A8 (shadow area of below diagram). Following is an example, which shows you how to define the base address as Hex 2C0.

Base Address : Hex 2C0

2		C				0			
1	1	1	1	0	0	0	0	0	0
A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

2.6 Interrupt Setting

The ACL-7124 provides 6 interrupt requests IRQ 2, 3, 4, 5, 6, and 7, which could be set for hardware interrupt generated by, I/O line, PC0 of Port C. The IRQ level is set by jumper J1, refer to figure 2.1 for its location.

Interrupt level : IRQ2

IRQ J1
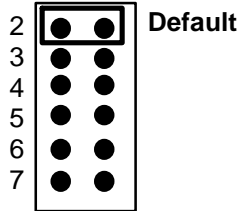
One of the three interrupt status of the ACL-7124 (DIS, PGM, and EN) should be set by jumper J2, please refer to Fig 2.3. The description of these interrupt status are :

DIS : the interrupt capability is always disabled.
EN : the interrupt capability is always enabled.
PGM : programmable interrupt.

If PGM is selected as interrupt status, the interrupt will be enabled when, I/O line, PC4 goes to TTL LOW. If the PC4 goes to TTL HIGH, then the interrupt will be disabled.
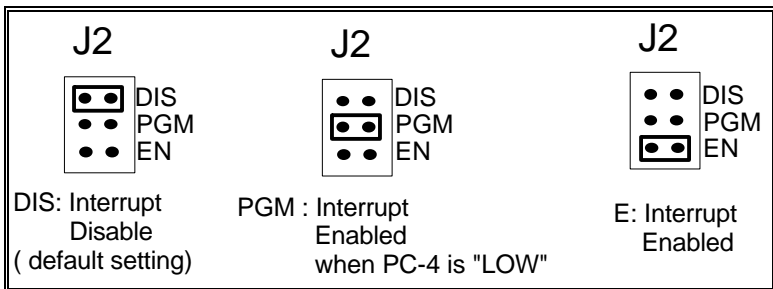
Figure 2.3 JP2 Jumper Setting

Two interrupt trigger edges : *rising* or *falling* are supported in the ACL-7124. It is selected by jumper J3, see the Fig 2.4 below.
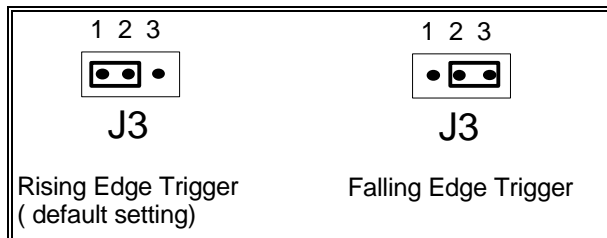
Fig 4.2 J3 jumper setting

A Summary of Interrupt Status

In ACL-7124, the interrupt trigger status are depended on jumper J2, and J3, and, I/O lines, PC0 and PC4. All the possibility of interrupt status are shown in the following table.

J2	J3	PC0	PC4	Interrupt Status
J2 (DIS / PGM / EN)	X	X	X	No Interrupt Request
J2 (DIS / PGM / EN)	J3 1 2 3	L -> H	X	Interrupt Request
J2 (DIS / PGM / EN)	J3 1 2 3	H -> L	X	Interrupt Request

J2 DIS PGM EN	J3 1 2 3	L -> H	LOW	Interrupt Request
J2 DIS PGM EN	J3 1 2 3	H -> L	LOW	Interrupt Request
J2 DIS PGM EN	X	X	High	No Interrupt Request

X : Don't Care
H-> L : Rising Edge Trigger (from High to Low)
L->H : Falling Edge Trigger (from Low to High)

2.7 Connector Pin Assignment

The I/O ports of ACL-7124 emulates as one mode 0 Intel 8255 general purpose programmable peripheral interface. Figure 2.4 shows ACL-7124's equally block diagram. One 50-pin connector come equipped with the ACL-7124 board, and it is corresponding to a mode 0 of 8255.

In addition, two 20-pin pin-head connectors are corresponding to the 50-pin connector. These two connectors are used to go with ACLD-785 and ACLD-782, which are 16 bit digital relay output board and digital opto-isolated input board, respectively.

The 50-pin connector's pin assignment is specified in Figure 2.5 below. The two 20-pin connectors' are specified in Figure 2.6 and Figure 2.7, respectively.

Figure 2.4

```
PC  7 ────────    1            2    ─────
PC  6 ────────    3            4    ─────
PC  5 ────────    5            6    ─────
PC  4 ────────    7            8    ─────
PC  3 ────────    9           10    ─────
PC  2 ────────   11           12    ─────
PC  1 ────────   13           14    ─────
PC  0 ────────   15           16    ─────
PB  7 ────────   17           18    ─────
PB  6 ────────   19           20    ─────
PB  5 ────────   21           22    ─────
PB  4 ────────   23           24    ─────
PB  3 ────────   25           26    ─────
PB  2 ────────   27           28    ─────
PB  1 ────────   29           30    ─────
PB  0 ────────   31           32    ─────
PA  7 ────────   33           34    ─────
PA  6 ────────   35           36    ─────
PA  5 ────────   37           38    ─────
PA  4 ────────   39           40    ─────
PA  3 ────────   41           42    ─────
PA  2 ────────   43           44    ─────
PA  1 ────────   45           46    ─────
PA  0 ────────   47           48    ─────
+5V   ────────   49           50    ─────
```
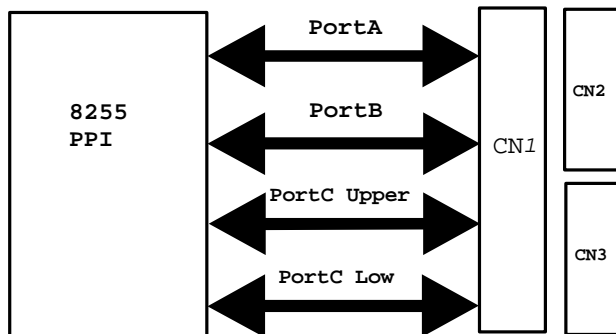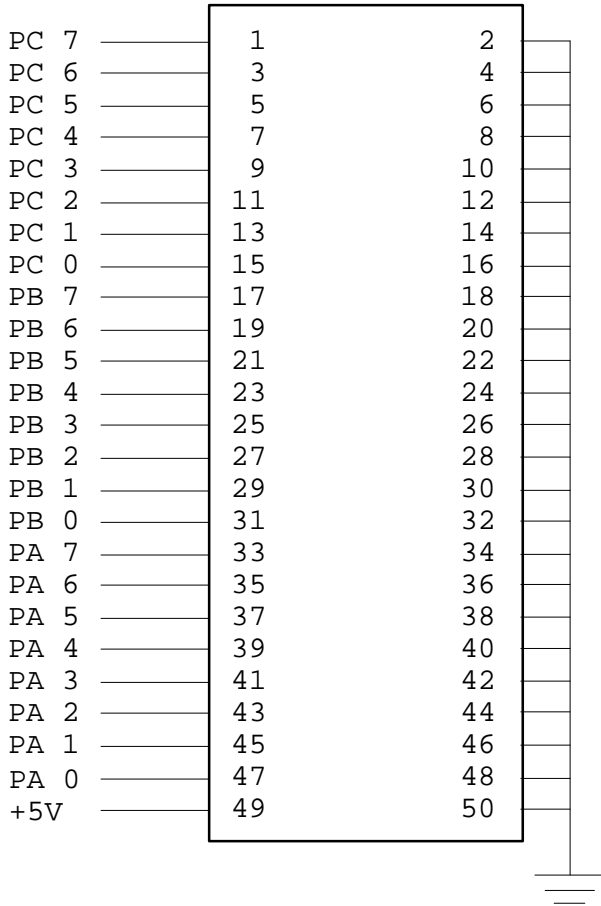
Figure 2.5 Connector Pin Assignment

- CN 2 : Port A & Port B

PA 0	1	2	PA 1
PA 2	3	4	PA 3
PA 4	5	6	PA 5
PA 6	7	8	PA 7
PB 0	9	10	PB 1
PB 2	11	12	PB 3
PB 4	13	14	PB 5
PB 6	15	16	PB 7
GND	17	18	GND
+5V	19	20	+5V
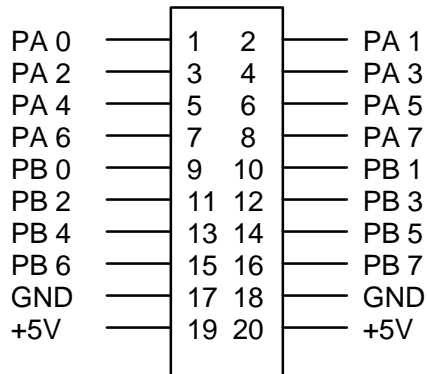
Figure 2.6 Pin Assignment of CN2

- CN 3 : Port C

PC 0	1	2	PC 1
PC 2	3	4	PC 3
PC 4	5	6	PC 5
PC 6	7	8	PC 7
NC	9	10	NC
NC	11	12	NC
NC	13	14	NC
NC	15	16	NC
GND	17	18	GND
+5V	19	20	+5V
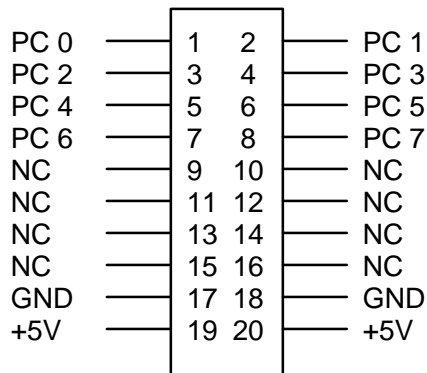
Figure 2.6 Pin Assignment of CN3

2.8 ACL-7124 Software Library Installation

The ACL-7124's software library supplied with ACL-7124 includes the utility software, C-language library and some demonstration programs which can help you reduce programming work.

1. Turn your PC's power switch on

2. Put the ADLink's "Manual & Software Utility" CD into the appropriate CD driver.

3. Type the commands(X indicates the CD ROM driver):

   X:\> **CD Software\Isa_Card\7124\DOS**
   X:\ Software\Isa_Card\7124\DOS> **SETUP**

4. An installation completed message will be shown on the screen.

After installation, all the files *of ACL-7124 Library & Utility for DOS* are stored in C:\ADLink\7124\DOS directory.

<h1>3</h1>

Programming

3.1 8255 Mode 0

The ACL-7124 can emulates MODE 0 of 8255 PPI, and it comes equipped with one 50-pin male IDC connectors that interface with OPTO-22 racks 8, 16, and 24.

The basic function definition of 8255 mode 0 is :

. Two 8-bit I/O ports – PA and PB
. Two nibble-wide (4-bit) ports – PC upper and PC lower
. Any ports can be used for both input and output
. Outputs are latched whereas inputs are not latched
. 16 different input/output configurations are available

Two, I/O lines, PC0 is used to generate a hardware interrupt, and PC4 is used to control programmable interrupt.

The I / O of ACL-7124 emulates as one 8255 programmable peripheral interface chip, the *c o n t r o l   w o r d* is to program PA, PB and PC as input port or output port. Table shows the summarize of control word (D0 – D4), and mode states (Mode 0 – Mode 15) .

```
D7 D6 D5 D4 D3 D2 D1 D0
```

| 1 | 0 | 0 | ? | ? | 0 | ? | ? |

```
                          1: input
                          0: output for Port C low nibbl

                          1: input
                          0: output for Port B

                          1: input
                          0: output for Port C high nibk

                          1: input
                          0: output for Port A
```
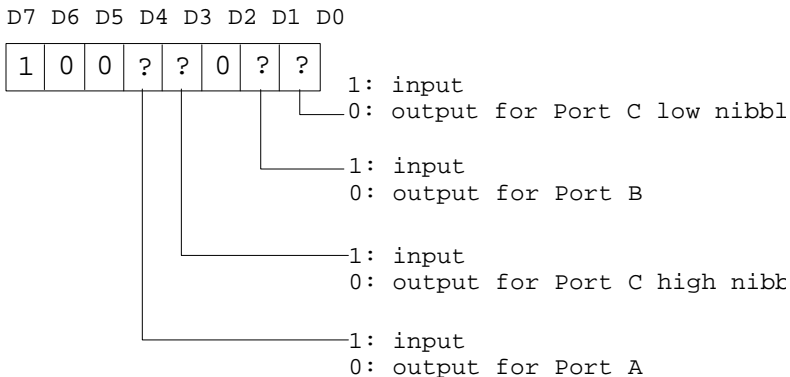
Config. Value	D4	D3	D1	D0	PORT A	PORT C UPPER	PORT B	PORT C LOWER
80H	0	0	0	0	O/P	O/P	O/P	O/P
81H	0	0	0	1	O/P	O/P	O/P	I/P
82H	0	0	1	0	O/P	O/P	I/P	O/P
83H	0	0	1	1	O/P	O/P	I/P	I/P
88H	0	1	0	0	O/P	I/P	O/P	O/P
89H	0	1	0	1	O/P	I/P	O/P	I/P
8AH	0	1	1	0	O/P	I/P	I/P	O/P
8BH	0	1	1	1	O/P	I/P	I/P	I/P
90H	1	0	0	0	I/P	O/P	O/P	O/P
91H	1	0	0	1	I/P	O/P	O/P	I/P
92H	1	0	1	0	I/P	O/P	I/P	O/P
93H	1	0	1	1	I/P	O/P	I/P	I/P
98H	1	1	0	0	I/P	I/P	O/P	O/P
99H	1	1	0	1	I/P	I/P	O/P	I/P
9AH	1	1	1	0	I/P	I/P	I/P	O/P
9BH	1	1	1	1	I/P	I/P	I/P	I/P

Table 4.1 Summarize of control word (D0 – D4) and mode state (Mode 0 – Mode 15)

3.2 Register Structure

The ACL−7124 needs 4 bytes of I/O address for I/O operations. The relationship of I/O address and ports' data read / write shows as following table (Table 4.2), the default base address of below table is 2C0H.

PORT SELECT	ADDR.	NOTE
PORT A	2C0H	EMULATE AS 8255 PA
PORT B	2C1H	EMULATE AS 8255 PB
PORT C	2C2H	EMULATE AS 8255 PC
CONTROL WORD (CFG)	2C3H	EMULATE AS 8255 CW

Table 4.2 Ports' I/O address table
(Base Address = 2C0H)

3.3 Interrupt Handling

The ACL−7124 can generate a hardware interrupt to your PC. The following issues should be careful when you want to generate an interrupt trigger.

1. Interrupt IRQ level setting : make sure you already set the right IRQ level by using the jumper J1. Please refer to section 2.7 "interrupt setting".

2. Interrupt trigger status setting :
   a. interrupt mode : make sure the jumper J2 is already set as $E\ N$ or $P\ G\ M$ mode.

   b. interrupt trigger edge : make sure what kind of edge trigger you need − rising or falling. Please set the jumper J2 for proper interrupt trigger edge.

   c. PGM mode: if you choice PGM mode, confirm the ,I/O line, PC4 is kept in TTL LOW status. Otherwise, there is no interrupt trigger will be occurred.

> **Note** : Since the ACL-7124's Input is not latched and no first event trapping is provided to determine which input was active first.

Self Interrupt Trigger

Although the ACL-7124's interrupt signals are normal received from external peripherals. It can also generate a test output signal to emulate an interrupt being inputted from an external device. An example program is shown in the section 3.5 for reference.

3.4 Programming Notes

Before programming the ACL-7124, the following notes will help you more skillful to control the I/O operations through the ACL-7124.

1. Default Input Mode :
    After power-on or hardware reset your PC system, all the ports of ACL-7124 are automatically configured as *I N P U T* mode.

2. Output Latch
    When an output port is programmed as output mode through control word, it will not affect the connected output device until an output instruction is executed. This means the data will not output until execute the first output instruction.
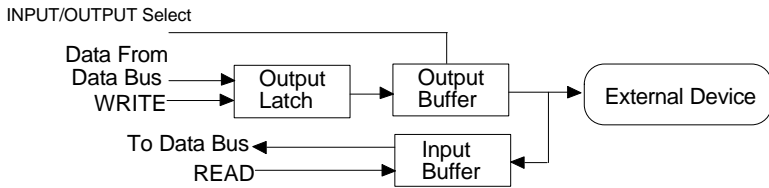
INPUT/OUTPUT Select

Data From
Data Bus ──→ | Output Latch | → | Output Buffer | → (External Device)
WRITE ──→

To Data Bus ←──
READ ────────→ | Input Buffer |

Figure 3.1 ACL-7124's Signal Direction

3. According the above ACL-7124's signal direction block diagram, some issues should be careful.
    a. When a port is set as INPUT or after hardware RESET, its output buffer is *D i s a b l e d*   (high impedance)

    b. The output data is lactated in the *O u t p u t   L a t c h* when it is set as OUTPUT mode.

    c. When the port is set as OUTPUT, the input circuit is used as an output status read-back.

    d. The data in Output Latch is an random value after power on. It has to be initialized before the port to output direction.

3.5 Programming in C language

The following parts are example programs written in C language. The first four parts are just partial programs for your reference, you can not compile them before these programs are complete.

The last program is an example for interrupt handling, you could compile it by Borland C/C++ compiler directly.

1. To initial I/O port

```
# define BASE 0x2C0      //define base address
# define CWD0 0x80        //0x80 refer to 8255 CW


    outportb( BASE + 3 , CWD);
                      // all ports as output */
    outportb( BASE + 0 , 0x00);
    outportb( BASE + 1 , 0x00);
    outportb( BASE + 2 , 0x00);
                      // PA, PB, and PC as 0x00
```

2. Write Data to Outport Ports

```
# define BASE 0x2C0      // define base address
# define PA   0x0        // Port A
# define PB   0x1        // Port B
# define PC   0x2        // Port C
# define CWD 0x80         //ALL output to 8255 CW


outportb(BASE + 3,CWD);  //index to CH0 CW
outportb(BASE + PA ,0x23);// write 23H to PA
outportb(BASE + PB ,0x45);// write 45H to PB
outportb(BASE + PC ,0xfd);// write fdH to PC
```

3. To Read Data from Input Ports

```
# define BASE 0x2C0      //define base address
# define PA   0x0        // Port A
# define PB   0x1        // Port B
# define PC   0x2        // Port C
# define CWD 0x9B        //ALL input from 8255 CW
int pa_data, pb_data, pc_data;

outportb(BASE + 3,CWD);  //index to CH0 CW
pa_d = inportb(BASE + PA); // read from PA
pb_d = inportb(BASE + PB); // read from PB
pc_d = inportb(BASE + PC); // read from PC
```

4. To Read Back from Output Ports

```
# define BASE 0x2C0      //define base address
# define PA   0x0        // Port A
# define PB   0x1        // Port B
# define PC   0x2        // Port C
# define CWD  0x80       //ALL input from 8255 CW
int pa_data, pb_data, pc_data;

outportb(BASE + 3,CWD);  //index to CH0 CW
outport( BASE + PA, 0xaa); // write 0xaa to PA
pa_d = inportb(BASE + PA); // read back from PA
if( pa_d != 0xaa)
{
    printf(" PortA read back error \n");
}

outport( BASE + PA, 0xaa); // write 0xbb to PB
pb_d = inportb(BASE + PB); // read back from PB
if( pa_d != 0xbb)
{
    printf(" PortB read back error \n");
}

outport( BASE + PA, 0xcc); // write 0xbb to PC
```

```
        pc_d = inportb(BASE + PC); // read from PC
        if( pa_d != 0xcc)
        {
            printf(" PortC read back error \n");
        }
```

5. A Complete Example Program for Interrupt Handling

```
/**************************************************/
 *   This program deno. how to generate interrupt by *
 *   the ACL-7124 itself. When you press any key, a   *
 *   beep is generated. When you press ESC key, the  *
 *   system will be quit.                             *
 *                                                    *
 *   Hardware setting :                               *
 *       Base Address : 0x2C0                         *
 *       IRQ Level    : 2  ( Jumper J1)               *
 *       Int mode     : EN ( jumper J2)               *
 *       edge trigger : 1-2 ( rising edge)            *
 **************************************************/

#include <stdio.h>
#include <dos.h>
#include <conio.h>

#define  IRQ2       0x0a
#define  EOI        0x20
#define  BASE_ADDR  0x2c0
#define  PA         0x00
#define  PB         0x01
#define  PC         0x02
#define  CW         0x03


void interrupt isr_7124()
{
    printf("\7");           // beep
    outportb( 0x20, EOI);   // EOI of 8259
}

main()
{
    int  mask, keyin;
```

```c
    void interrupt (*old_irq2_isr)();

    old_irq2_isr = getvect( IRQ2);
    setvect( IRQ2, isr_7124);
    mask = inportb( 0x21);

    outportb( BASE_ADDR + CW, 0x80);  // set PA, PB and PC
                                      // as output mode
    clrscr();                         // clear screen
    printf( " press <ESC> to QUIT \n");
    do
    {
       keyin = 0;
       printf(" press any key to genetate an interrupt
                 except <ESC>\n" );
       keyin = bioskey(0);

       outportb( 0x21, 0xbf & mask); // IRQ2 nonmasked

       outportb( BASE_ADDR + PC, 0x00);
       delay( 100);
       outportb( BASE_ADDR + PC, 0x01);

    } while( (keyin & 0xff) != 27); // QUIT when ESC pressed

    setvect( IRQ2, old_irq2_isr);   // restore old isr
    outportb( 0x21, mask);          // restore 8259 mask
}
```

Appendix A. I/O Port Address Map

I/O Address	Device
000-01F	DMA controller 1
020–03F	interrupt controller
040–05F	Timer
060–06F	Keyboard
070–07F	Real–time clock
080–09F	DMA page register
0A0–0BF	Interrupt controller 2
0C0–0DF	DMA controller
0F0–0FF	Math coprocessor
100–1EF	not usable
1F0–1F8	Fixed disk
200–207	Game I/O
278–27F	Parallel printer port 2 (LPT2:)
2F8–2FF	Serial Port 2 (COM2:)
300–31F	Prototype card
360–36F	Reserved
378–37F	Parallel printer port 1 (LPT1:)
3B0–3BF	Monochrome display
3C0–3CF	Reserved
3D0–3DF	Color graphics display
3F0–3F7	Diskette controller
3F8–3FF	Serial port 1 (COM 1:)

Product Warranty/Service

Seller warrants that equipment furnished will be free form defects in material and workmanship for a period of one year from the confirmed date of purchase of the original buyer and that upon written notice of any such defect, Seller will, at its option, repair or replace the defective item under the terms of this warranty, subject to the provisions and specific exclusions listed herein.
This warranty shall not apply to equipment that has been previously repaired or altered outside our plant in any way as to, in the judgment of the manufacturer, affect its reliability. Nor will it apply if the equipment has been used in a manner exceeding its specifications or if the serial number has been removed.
Seller does not assume any liability for consequential damages as a result from our products uses, and in any event our liability shall not exceed the original selling price of the equipment.
The equipment warranty shall constitute the sole and exclusive remedy of any Buyer of Seller   equipment and the sole and exclusive liability of the Seller, its successors or assigns, in connection with equipment purchased and in lieu of all other warranties expressed implied or statutory, including, but not limited to, any implied warranty of merchant ability or fitness and all other obligations or liabilities of seller, its successors or assigns.
The equipment must be returned postage-prepaid. Package it securely and insure it. You will be charged for parts and labor if you lack proof of date of purchase, or if the warranty period is expired.